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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/530,661	09/20/1995	BRENT KEETH	MI22-356	5492

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EXAMINER	
WILLE, DOUGLAS A	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/530,661	KEETH ET AL.	
	Examiner	Art Unit	
	Douglas A Wille	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10,18,19,22,23,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10,18,19,22,23,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0803*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6 – 10, 18, 19, 22, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. ('038) in view of Eimore, Nakamura et al. and Takahashi et. al. ('000).

3. With respect to claim 6, Takahashi et al. ('038) shows (see cover Figure and column 8, line 17 et seq.) a DRAM device where the cell size is $6F^2$ (column 25, line 17) but does not show the minimum feature size, peripheral circuitry, array size or packaging. Eimore shows (see cover figure and column 8, line 9) a DRAM (column 1, line 9) where a 0.25 micron design rule is used (column 10, line 61). Nakamura et al. shows a DRAM (see cover Figure and column 3, line 66 et seq.) where a 16 M device is shown (column 4, line 25) and shows the chip includes, besides the memory array, timing, address, redundancy, data, test path and voltage supply circuitry. Takahashi et al. ('000) show (see Figure 1 and column 5, line 67 et seq.) a DRAM (column 6, line 10) where the die is encapsulated in a package with pins extending outwardly. It would have been obvious to include the peripheral circuitry show by Nakamura et al. since it provides a working device, to include the feature size shown by Eimore since it is known to be functional and to provide a 16M device since it is known to be useful. Note that with the 0.25 micron design rule the area of the memory is less than 6 mm^2.

4. With respect to claim 7, the memory array is shown by Takashima et al. ('038) as 4-level (see Figure 29 and column 26, line 34 et seq.) and since the peripheral circuitry does not have an integrated capacitor, it would inherently have less than 4-levels.

5. With respect to claim 8, Nakamura et al. show that Figure 1 matches the geometric arrangement of the actual chip and with the memory area being less than 6 mm^2, the whole chip will obviously be less than 35 mm^2.

6. With respect to claim 9, Takahashi et al. ('038) shows a structure with 5-levels (see Figure 47 and column 28, line 63 et seq.) and since the peripheral circuitry does not have an integrated capacitor, it would inherently have less than 5-levels. Also the memory will have an area of less than 6 mm^2.

7. With respect to claim 10, Nakamura et al. show that Figure 1 matches the geometric arrangement of the actual chip and with the memory area being less than 6 mm^2, the whole chip will obviously be less than 35 mm^2 and Takahashi et al. ('038) shows a structure with 5-levels (see Figure 47 and column 28, line 63 et seq.) and since the peripheral circuitry does not have an integrated capacitor, it would inherently have less than 5-levels. Also the memory will have an area of less than 6 mm^2.

8. With respect to claims 18, 19 and 25, the memory arrays with the density shown will have 270 devices in 100 $micron^2$.

9. With respect to claims 22, 23 and 26, the 16M device has no more than 68M memory cells and with the density shown will have 270 devices in 100 $micron^2$.

Response to Arguments

10. Applicant's arguments filed 7/11/03 have been fully considered but they are not persuasive.

11. Applicant states that the references cannot be combined and do not show the claimed device but as described above, Eimore shows that a specific feature size can be realized and since the feature size is not shown by Takahashi et al. it would be obvious to use Eimore to size the device. It is noted that all the claimed features are shown by the combined references as shown above.

12. Applicant states that there are oxidation issues and bit line spacing issues but these features are shown by Eimore and are successful.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A Wille whose telephone number is (571) 272-1721. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Douglas A. Wille
Primary Examiner

January 20, 2004